UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,623	08/05/2003	Kazunori Sakurai	105943.01	5364

25944 7590 03/18/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WOOD, KEVIN S	
ART UNIT	**PAPER NUMBER**
2874	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,623	SAKURAI ET AL.	
	Examiner	Art Unit	
	Kevin S Wood	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0803.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Brian Healy
Primary Examiner

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,989,934 to Zavracky et al.

Referring to claim 1, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses an optical module including: an optical waveguide (70,72); an optical element (35) having an optical section; a semiconductor chip (10) electrically connected to the optical element; a substrate (82) having a first surface (top) and a second surface (bottom), the substrate supporting the semiconductor chip and the optical element on the first surface; an interconnect pattern formed on the first surface, the interconnect pattern electrically connected to the semiconductor chip; and external terminals (PIN) provided over the second surface, the external terminals electrically connected to the interconnect pattern. See Fig. 1(a) through Fig. 5, along with their respective portions of the specification.

Referring to claim 2, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses the substrate having through holes formed therein to electrically connect the external terminals to the interconnect pattern. See Fig. 4(b).

Referring to claim 3, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses that the optical element (35) and the semiconductor chip (10) are packaged (102). See Fig. 4(b).

Referring to claim 5, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses the semiconductor chip (10) and the substrate (82) having first and second holes formed therein and overlapped with each other; whereing the optical waveguide (72) is inserted into the first and second holes; and wherein the optical element (35) is disposed so that the optical section and one end surface of the inserted optical waveguide are opposed. See Fig. 4(b).

Referring to claim 7, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses the semiconductor chimp has an internal circuit (20) for driving the optical element (20,35). See Fig. 1(a) through 4(b).

Referring to claim 8, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses the optical element (35) and the semiconductor chip are stacked. See Fig. 4(b).

Referring to claim 9, Zavracky et al. discloses all the limitations of the claimed invention. Zavracky et al. discloses the interconnect patter is connected to the optical element. See Fig. 4(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,989,934 to Zavracky et al. in view of U.S. Patent No. 6,301,401 to La.

Referring to claim 4, Zavracky et al. discloses all the limitations of the claimed invention, except Zavracky et al. does not appear to disclose a resin being used to package the semiconductor chip and the optical element. La discloses an optical module that is similar to the claimed invention. La discloses the use of a resin (190) for the purpose of packaging the optical and electrical components of the optical module. Since Zavracky et al. and La are both from the same field of endeavor; the purpose disclosed by La would have been recognized in the pertinent art of Zavracky et al. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a resin for packaging the components with in the optical module

disclosed by Zavracky et al., since it was known within the art that resins can be used to package optical components, in order to protect them from the environment and to make the packages durable.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,989,934 to Zavracky et al. in view of U.S. Patent No. 6,100,595 to Jaouen et al.

Referring to claim 4, Zavracky et al. discloses all the limitations of the claimed invention, except Zavracky et al. does not appear to disclose a transparent underfill material provided between the optical element and the semiconductor chip. Jaouen et al. discloses an optical module that is similar to the claimed invention. Jaouen et al. discloses the use the use of an underfill material to couple the waveguide to the chip (2) and package (3), for the purpose of forming a stronger mechanical bond between the components. Since Zavracky et al. and Jaouen et al. are both from the same field of endeavor; the purpose disclosed by Jaouen et al. would have been recognized in the pertinent art of Zavracky et al. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize an underfill material for coupling the waveguide with the chip and the substrate, since it was known in the art that an underfill material helps to increase the bond strength between the components and helps to seal the connection between the components so that no undesired particles or debris can end up between the waveguide and the optical element, causing undesired optical loses.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin S Wood whose telephone number is (571) 272-2364. The examiner can normally be reached on Monday-Thursday (7am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney B Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KSW

Brian Healy
Primary Examiner